Consider the function $Y = [A \overline{(B + C D)}]$. The $\overline{}$ indicates NOT.

1. Draw the CMOS schematic for $Y$, with inputs $A$, $B$, $C$ and $D$ and output $Y$.

2. Show the waveforms to perform the functional testing of the circuit.

3. Draw the Karnaugh map and indicate the transitions on the output signal caused by a single input.

4. Draw the waveforms to perform the delay testing of the circuit using the results from 3. Indicate where the delays should be measured.

5. For the case when $A = B = C = H$ and you are measuring the delay from $D$ to $Y$, indicate on the schematic how the toggle of the $D$ input turns the paths through the NMOS and PMOS transistors ON and OFF.

Homework assignments are in the Class Folder and on the web page, http://jan.ucc.nau.edu/~ejb3/ee482