1. Consider the full adder with inputs $a$, $b$, $ci$ and outputs $co$ and $s$.

   a) Show the waveforms to perform the functional testing of the circuit.

   a

   b

   ci

   co

   s

   b) Draw the waveforms to perform the delay testing of the circuit. Indicate where the delays should be measured.

   These waveforms show the delays for $a$ to $s$ and $a$ to $co$. For the $b$ to $s$ and $b$ to $co$ waveforms, switch the $a$ and $b$ waveforms. For the $ci$ to $s$ and $ci$ to $co$ waveforms, switch the $a$ and $ci$ waveforms.
2. Consider the flip-flop with synchronous set. The inputs are \( d, \text{ clk}, \) and \( \text{ set}. \) The output is \( q. \)

a) Show the waveforms to perform the functional testing of the circuit.

Since the flip-flop is a sequential circuit, the output depends on previous inputs (which means the Karnaugh map is meaningless). So you must test the functionality of each signal. The first part shows clocking in a HIGH, then clocking in a LOW on the positive edge of the clock. Then, after clocking in a HIGH, the clrb signal is asserted and \( q \) goes LOW. Notice that clrb holds off clocking in a HIGH and the output remains LOW even after clrb goes HIGH. Then the output goes HIGH on the next positive clock edge when the data is HIGH.

b) Draw the waveforms to perform the delay testing of the circuit. Indicate where the delays should be measured.
The delays to be measured are the clk -> q, both $t_{PLH}$ and $t_{PHL}$. These are shown on the function test above. The other delay is set -> q. There are 4 possible conditions for d and clk. These 4 tests are shown below.

Note there are several other timing measurements that we are not performing: minimum pulse width (clk and set) and setup and hold (data to clk).

Homework assignments are in the Class Folder and on the web page, [http://jan.ucc.nau.edu/~ejb3/ee482](http://jan.ucc.nau.edu/~ejb3/ee482)